

## CD4066B CMOS Quad Bilateral Switch

### 1 Features

- 15-V Digital or  $\pm 7.5$ -V Peak-to-Peak Switching
- 125- $\Omega$  Typical On-State Resistance for 15-V Operation
- Switch On-State Resistance Matched to Within 5  $\Omega$  Over 15-V Signal-Input Range
- On-State Resistance Flat Over Full Peak-to-Peak Signal Range
- High On or Off Output-Voltage Ratio: 80 dB Typical at  $f_{is} = 10$  kHz,  $R_L = 1$  k $\Omega$
- High Degree of Linearity: <0.5% Distortion Typical at  $f_{is} = 1$  kHz,  $V_{is} = 5$ -V<sub>p-p</sub>,  $V_{DD} - V_{SS} \geq 10$ -V,  $R_L = 10$  k $\Omega$
- Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at  $V_{DD} - V_{SS} = 10$ -V,  $T_A = 25^\circ\text{C}$
- Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit):  $10^{12}$   $\Omega$  Typical
- Low Crosstalk Between Switches: -50 dB Typical at  $f_{is} = 8$  MHz,  $R_L = 1$  k $\Omega$
- Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch On = 40 MHz Typical
- 100% Tested for Quiescent Current at 20-V
- 5-V, 10-V, and 15-V Parametric Ratings

### 2 Applications

- Analog Signal Switching and Multiplexing: Signal Gating, Modulators, Squelch Controls, Demodulators, Choppers, Commutating Switches
- Digital Signal Switching and Multiplexing
- Transmission-Gate Logic Implementation
- Analog-to-Digital and Digital-to-Analog Conversions
- Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain
- [Building Automation](#)

### 3 Description

The CD4066B device is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B device, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

The CD4066B device consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in [Figure 17](#), the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to  $V_{SS}$  (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

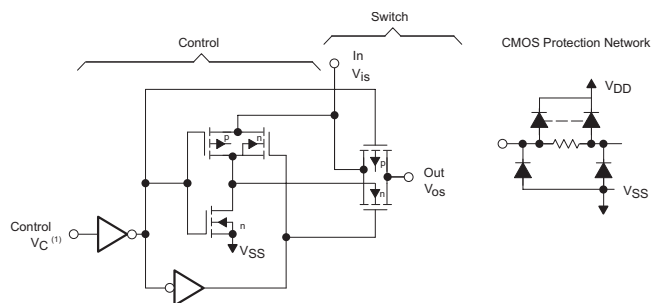
The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B device is recommended.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD4066B	PDIP (14)	19.30 mm x 6.35 mm
	CDIP (14)	19.50 mm x 6.92 mm
	SOIC (14)	8.65 mm x 3.91 mm
	SOP (14)	10.30 mm x 5.30 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Bidirectional Signal Transmission Via Digital Control Logic

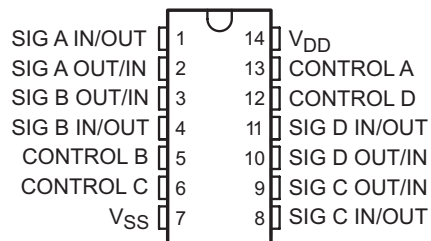


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## 5 Pin Configuration and Functions

**N, J, D, NS, or PW Packages  
14-Pin PDIP, CDIP, SOIC, SO, or TSSOP  
Top View**



**Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SIG A IN/OUT	I/O	Input/Output for Switch A
2	SIG A OUT/IN	I/O	Output/Input for Switch A
3	SIG B OUT/IN	I/O	Output/Input for Switch B
4	SIG B IN/OUT	I/O	Input/Output for Switch B
5	CONTROL B	I	Control pin for Switch B
6	CONTROL C	I	Control pin for Switch C
7	V <sub>SS</sub>	—	Low Voltage Power Pin
8	SIG C IN/OUT	I/O	Input/Output for Switch C
9	SIG C OUT/IN	I/O	Output/Input for Switch C
10	SIG D OUT/IN	I/O	Output/Input for Switch D
11	SIG D IN/OUT	I/O	Input/Output for Switch D
12	CONTROL D	I	Control Pin for D
13	CONTROL A	I	Control Pin for A
14	V <sub>DD</sub>	—	Power Pin