CD405xB CMOS Single 8-Channel Analog Multiplexer or Demultiplexer With Logic-Level Conversion

1 Features

- Wide range of digital and analog signal levels:
  - Digital: 3 V to 20 V
  - Analog: ≤ 20 V_{P-P}
- Low ON resistance, 125 Ω (typical) over 15 V_{P-P} signal input range for $V_{DD} – V_{EE}$ = 18 V
- High OFF resistance, channel leakage of ±100 pA (typical) at $V_{DD} – V_{EE}$ = 18 V
- Logic-level conversion for digital addressing signals of 3 V to 20 V ($V_{DD} – V_{SS}$ = 3 V to 20 V) to switch analog signals to 20 V_{P-P} ($V_{DD} – V_{EE}$ = 20 V) matched switch characteristics, r_{ON} = 5 Ω (typical) for $V_{DD} – V_{EE}$ = 15 V very low quiescent power dissipation under all digital-control input and supply conditions, 0.2 µW (typical) at $V_{DD} – V_{SS} = V_{DD} – V_{EE}$ = 10 V
- Binary address decoding on chip
- 5 V, 10 V, and 15 V parametric ratings
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package temperature range, 100 nA at 18 V and 25°C
- Break-before-make switching eliminates channel overlap

2 Applications

- Analog and digital multiplexing and demultiplexing
- Analog to digital and digital to analog conversion
- Signal gating
- Factory automation
- Televisions
- Appliances
- Consumer audio
- Programmable logic circuits
- Sensors

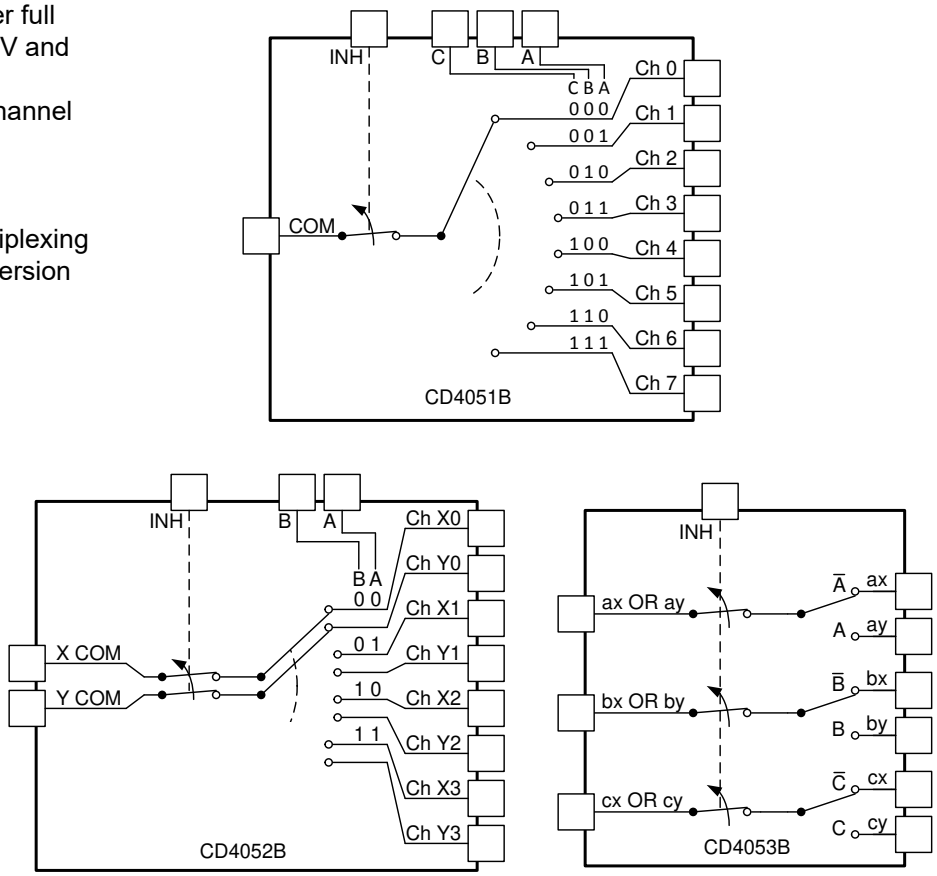
3 Description

The CD405xB analog multiplexers and demultiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} – V_{SS}$ and $V_{DD} – V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD405xB	J (CDIP, 16)	19.50 mm × 6.92 mm
	N (PDIP, 16)	19.30 mm × 6.35 mm
	D (SOIC, 16)	9.90 mm × 3.91 mm
	NS (SOP, 16)	10.30 mm × 5.30 mm
	PW (TSSOP, 16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Diagrams of CD405xB

5 Pin Configuration and Functions

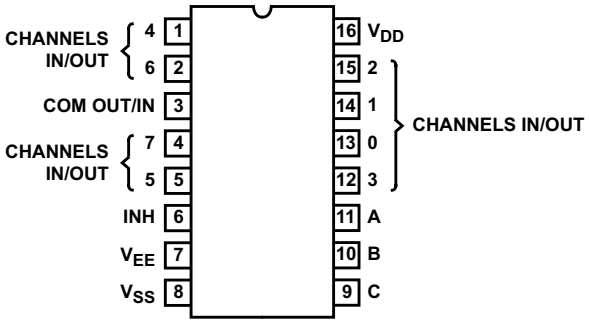


Figure 5-1. CD4051B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP (Top View)

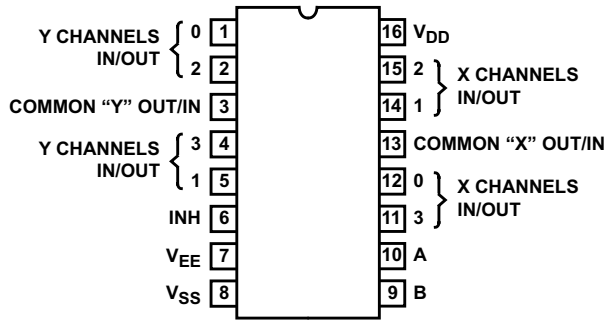


Figure 5-2. CD4052B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOP, and TSSOP (Top View)

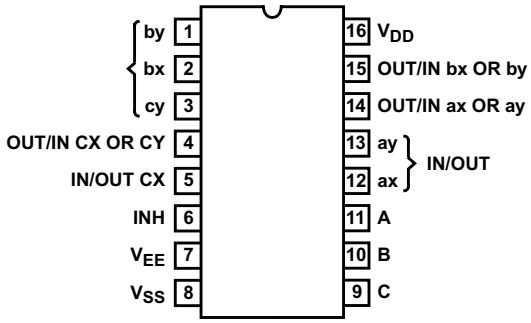


Figure 5-3. CD4053B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOP, and TSSOP (Top View)

Table 5-1. Pin Functions CD4051B

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	CH 4 IN/OUT	I/O	Channel 4 in/out
2	CH 6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH 7 IN/OUT	I/O	Channel 7 in/out
5	CH 5 IN/OUT	I/O	Channel 5 in/out
6	INH	I	Disables all channels. See Table 8-1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	C	I	Channel select C. See Table 8-1.
10	B	I	Channel select B. See Table 8-1.
11	A	I	Channel select A. See Table 8-1.
12	CH 3 IN/OUT	I/O	Channel 3 in/out
13	CH 0 IN/OUT	I/O	Channel 0 in/out
14	CH 1 IN/OUT	I/O	Channel 1 in/out
15	CH 2 IN/OUT	I/O	Channel 2 in/out
16	V_{DD}	—	Positive power input

(1) I = input, O = output