CD4013B CMOS Dual D-Type Flip-Flop

1 Features

- Asynchronous Set-Reset Capability
- Static Flip-Flop Operation
- Medium-Speed Operation: 16 MHz (Typical) Clock Toggle Rate at 10-V Supply
- Standardized Symmetrical Output Characteristics
- Maximum Input Current Of 1-µA at 18 V Over Full Package Temperature Range:
  - 100 nA at 18 V and 25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V

2 Applications

- Power Delivery
- Grid Infrastructure
- Medical, Healthcare, and Fitness
- Body Electronics and Lighting
- Building Automation
- Telecom Infrastructure
- Test and Measurement

3 Description

The CD4013B device consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

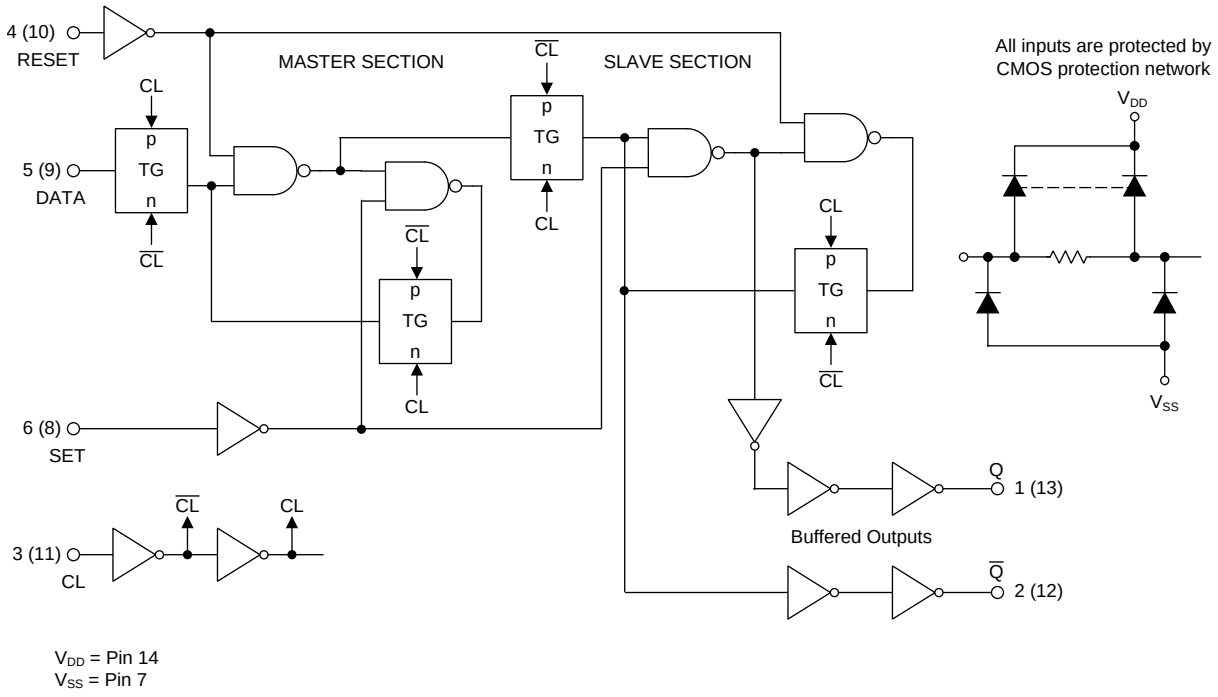
The CD4013B types are supplied in 14-pin dual-in-line plastic packages (E suffix), 14-pin small-outline packages (M, MT, M96, and NSR suffixes), and 14-pin thin shrink small-outline packages (PW and PWR suffixes).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD4013BE	PDIP (14)	19.30 mm x 6.35 mm
CD4013BF	CDIP (14)	19.50 mm x 6.92 mm
CD4013BM	SOIC (14)	8.65 mm x 3.90 mm
CD4013BNS	SO (14)	10.20 mm x 5.30 mm
CD4013BPW	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

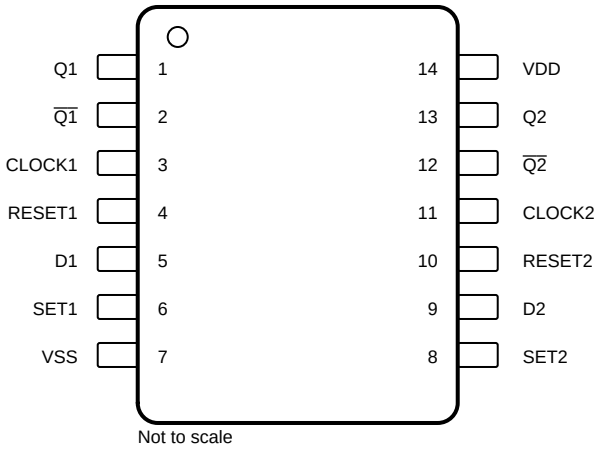
Logic Diagram



V_{DD} = Pin 14
V_{SS} = Pin 7

5 Pin Configuration and Functions

D, J, N, NS, PW Package
14-Pin SOIC, CDIP, PDIP, SO, TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Q1	O	Channel 1 output
2	$\overline{Q1}$	O	Inverted channel 1 output
3	CLOCK1	I	Channel 1 clock input
4	RESET1	I	Channel 1 reset
5	D1	I	Channel 1 data input
6	SET1	I	Channel 1 set
7	V_{SS}	—	Ground
8	SET2	I	Channel 2 set
9	D2	I	Channel 2 data input
10	RESET2	I	Channel 2 reset
11	CLOCK2	I	Channel 2 clock input
12	$\overline{Q2}$	O	Inverted channel 2 output
13	Q2	O	Channel 2 output
14	V_{DD}	—	Power supply