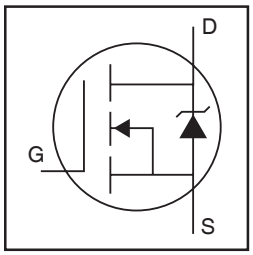
International
IOR Rectifier

IRFB4110PbF

HEXFET® Power MOSFET

Applications

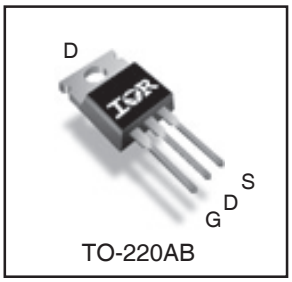
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}	100V
$R_{DS(on)}$ typ.	3.7mΩ
max.	4.5mΩ
I_D (Silicon Limited)	180A ①
I_D (Package Limited)	120A

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead Free
- RoHS Compliant, Halogen-Free



TO-220AB

G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB4110PbF	TO-220	Tube	50	IRFB4110PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, VGS @ 10V (Silicon Limited)	180①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	130①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	120	
I_{DM}	Pulsed Drain Current ②	670	
P_D @T_C = 25°C	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	5.3	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	190	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	—	0.402	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧	—	62	

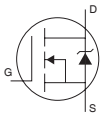
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.108	—	V/°C	Reference to 25°C, I_D = 5mA②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.7	4.5	mΩ	V_{GS} = 10V, I_D = 75A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	160	—	—	S	V_{DS} = 50V, I_D = 75A
Q_g	Total Gate Charge	—	150	210	nC	I_D = 75A
Q_{gs}	Gate-to-Source Charge	—	35	—		V_{DS} = 50V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	43	—		V_{GS} = 10V ⑤
R_G	Gate Resistance	—	1.3	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	V_{DD} = 65V
t_r	Rise Time	—	67	—		I_D = 75A
$t_{d(off)}$	Turn-Off Delay Time	—	78	—		R_G = 2.6Ω
t_f	Fall Time	—	88	—		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	—	9620	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	670	—		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	—	250	—		f = 1.0MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)⑦	—	820	—		V_{GS} = 0V, V_{DS} = 0V to 80V ⑧
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑥	—	950	—		V_{GS} = 0V, V_{DS} = 0V to 80V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	170①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②⑦	—	—	670		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 75A, V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	—	50	75	ns	T_J = 25°C V_R = 85V,
		—	60	90		T_J = 125°C I_F = 75A
Q_{rr}	Reverse Recovery Charge	—	94	140	nC	T_J = 25°C di/dt = 100A/µs ⑤
		—	140	210		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	3.5	—	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.033mH R_G = 25Ω, I_{AS} = 108A, V_{GS} =10V. Part not recommended for use above this value.

④ I_{SD} ≤ 75A, di/dt ≤ 630A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑨ R_θ is measured at T_J approximately 90°C.