

MJE13003

SWITCHMODE™ Series NPN Silicon Power Transistor

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

Features

- Reverse Biased SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 0.5 to 1.5 A, 25 and 100°C
 t_c @ 1 A, 100°C is 290 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Pb-Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(\text{sus})}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current – Continuous – Peak (Note 1)	I_C I_{CM}	1.5 3	Adc
Base Current – Continuous – Peak (Note 1)	I_B I_{BM}	0.75 1.5	Adc
Emitter Current – Continuous – Peak (Note 1)	I_E I_{EM}	2.25 4.5	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.4 11.2	W mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40 320	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J , T_{stg}	–65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.12	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	89	$^\circ\text{C}/\text{W}$
Maximum Load Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

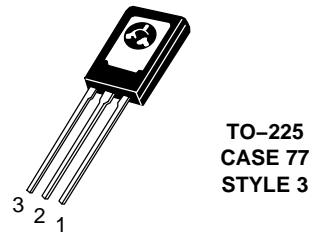
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

<http://onsemi.com>

**1.5 AMPERES
NPN SILICON POWER
TRANSISTORS
300 AND 400 VOLTS
40 WATTS**



TO-225
CASE 77
STYLE 3

MARKING DIAGRAM



Y = Year
WW = Work Week
JE13003 = Device Code
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE13003	TO-225	500 Units/Box
MJE13003G	TO-225 (Pb-Free)	500 Units/Box

MJE13003

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)					
Collector-Emitter Sustaining Voltage ($I_C = 10 \text{ mA}, I_B = 0$)	$V_{CEO(\text{sus})}$	400	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(\text{off})} = 1.5 \text{ Vdc}$) (V_{CEV} = Rated Value, $V_{BE(\text{off})} = 1.5 \text{ Vdc}, T_C = 100^\circ\text{C}$)	I_{CEV}	– –	– –	1 5	mAdc
Emitter Cutoff Current ($V_{EB} = 9 \text{ Vdc}, I_C = 0$)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			–
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 12			–
ON CHARACTERISTICS (Note 2)					
DC Current Gain ($I_C = 0.5 \text{ Adc}, V_{CE} = 2 \text{ Vdc}$) ($I_C = 1 \text{ Adc}, V_{CE} = 2 \text{ Vdc}$)	h_{FE}	8 5	– –	40 25	–
Collector-Emitter Saturation Voltage ($I_C = 0.5 \text{ Adc}, I_B = 0.1 \text{ Adc}$) ($I_C = 1 \text{ Adc}, I_B = 0.25 \text{ Adc}$) ($I_C = 1.5 \text{ Adc}, I_B = 0.5 \text{ Adc}$) ($I_C = 1 \text{ Adc}, I_B = 0.25 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{CE(\text{sat})}$	– – – –	– – – –	0.5 1 3 1	Vdc
Base-Emitter Saturation Voltage ($I_C = 0.5 \text{ Adc}, I_B = 0.1 \text{ Adc}$) ($I_C = 1 \text{ Adc}, I_B = 0.25 \text{ Adc}$) ($I_C = 1 \text{ Adc}, I_B = 0.25 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{BE(\text{sat})}$	– – –	– – –	1 1.2 1.1	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product ($I_C = 100 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1 \text{ MHz}$)	f_T	4	10	–	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$)	C_{ob}	–	21	–	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Delay Time		t_d	–	0.05	0.1
Rise Time	($V_{CC} = 125 \text{ Vdc}, I_C = 1 \text{ A}, I_{B1} = I_{B2} = 0.2 \text{ A}, t_p = 25 \mu\text{s}$, Duty Cycle $\leq 1\%$)	t_r	–	0.5	1
Storage Time		t_s	–	2	4
Fall Time		t_f	–	0.4	0.7
Inductive Load, Clamped (Table 1, Figure 13)					
Storage Time	($I_C = 1 \text{ A}, V_{clamp} = 300 \text{ Vdc}, I_{B1} = 0.2 \text{ A}, V_{BE(\text{off})} = 5 \text{ Vdc}, T_C = 100^\circ\text{C}$)	t_{sv}	–	1.7	4
Crossover Time		t_c	–	0.29	0.75
Fall Time		t_{fi}	–	0.15	–

2. Pulse Test: $PW = 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

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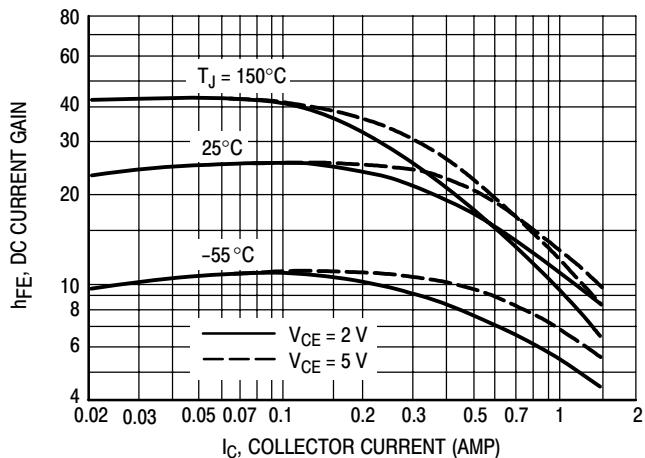


Figure 1. DC Current Gain

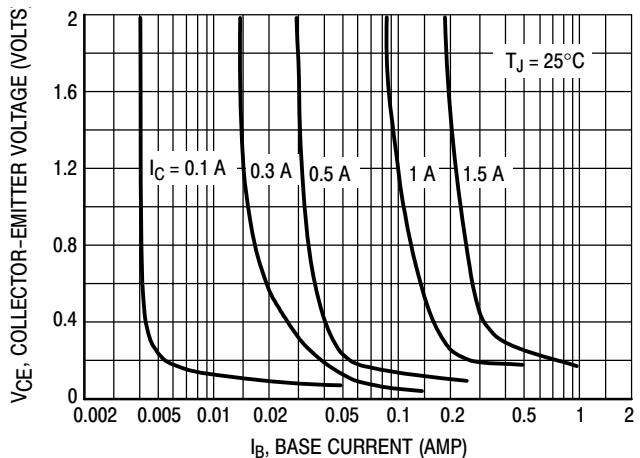


Figure 2. Collector Saturation Region

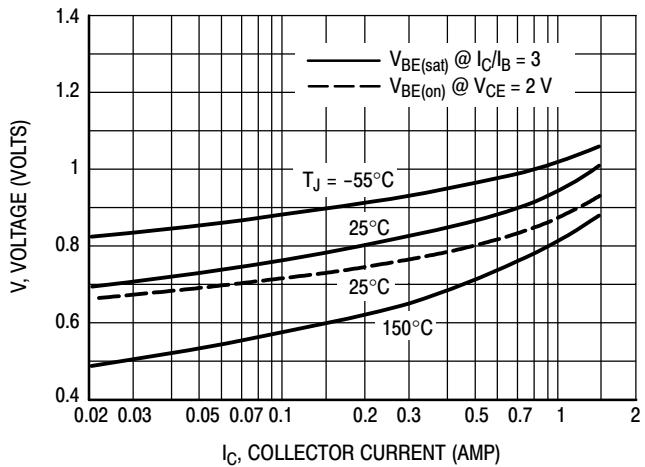


Figure 3. Base-Emitter Voltage

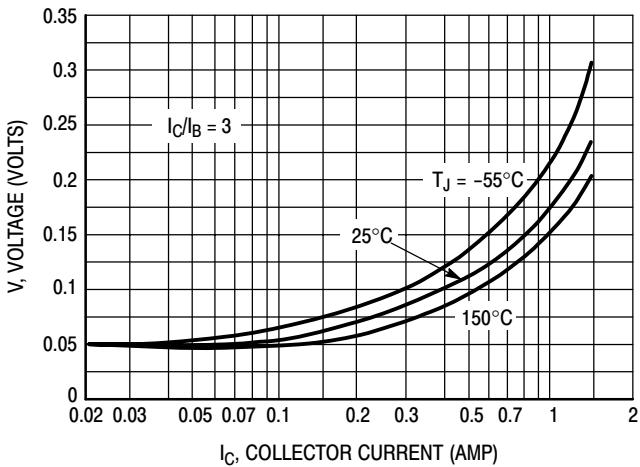


Figure 4. Collector-Emitter Saturation Region

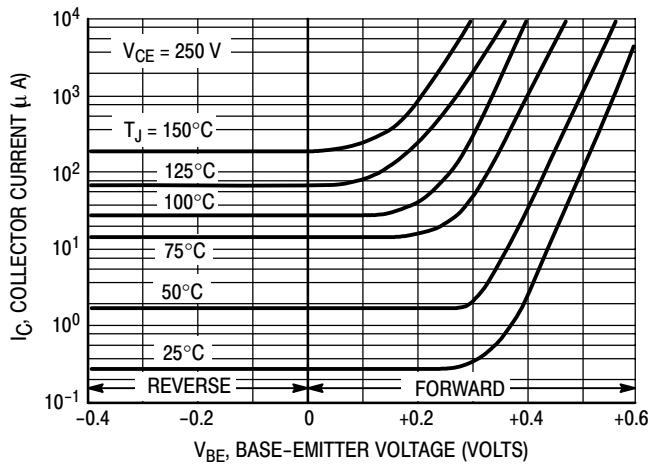


Figure 5. Collector Cutoff Region

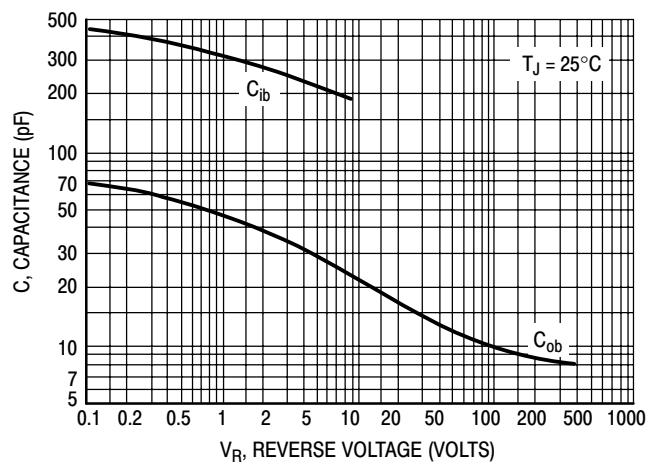


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING	
TEST CIRCUITS	<p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_B</p> <p>*SELECTED FOR ≥ 1 kV</p>		
CIRCUIT VALUES	<p>Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20</p> <p>GAP for 30 mH/2 A $L_{coil} = 50$ mH</p>	<p>V_{CC} = 20 V $V_{clamp} = 300$ Vdc</p>	<p>V_{CC} = 125 V $R_C = 125 \Omega$ D1 = 1N5820 or Equiv. $R_B = 47 \Omega$</p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil} (I_C_{pk})}{V_{CC}}$</p> <p>$t_2 \approx \frac{L_{coil} (I_C_{pk})}{V_{clamp}}$</p> <p>Test Equipment Scope—Tektronics 475 or Equivalent</p>	<p>$t_f, t_2 < 10$ ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p>	