

MJE13009

Preferred Device

SWITCHMODE™ Series NPN Silicon Power Transistors

The MJE13009 is designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

Features

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 3 to 12 Amp, 25 and $100^\circ\text{C } t_c$ @ 8 A, 100°C is 120 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Pb-Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	700	Vdc
Emitter-Base Voltage	V_{EBO}	9	Vdc
Collector Current – Continuous	I_C	12	Adc
– Peak (Note 1)	I_{CM}	24	
Base Current – Continuous	I_B	6	Adc
– Peak (Note 1)	I_{BM}	12	
Emitter Current – Continuous	I_E	18	Adc
– Peak (Note 1)	I_{EM}	36	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	2 16	W W/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	100 800	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.25	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

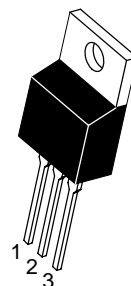
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

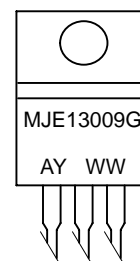
<http://onsemi.com>

**12 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS – 100 WATTS**



TO-220AB
CASE 221A-09
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE13009	TO-220	50 Units / Rail
MJE13009G	TO-220 (Pb-Free)	50 Units / Rail

Preferred devices are recommended choices for future use and best overall value.

MJE13009

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (Note 2)

Collector-Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	400	–	–	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	– –	– –	1 5	mAdc
Emitter Cutoff Current ($V_{EB} = 9\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	–	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased Clamped Inductive SOA with Base Reverse Biased	$I_{S/b}$ –	See Figure 1 See Figure 2			
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ON CHARACTERISTICS (Note 2)

DC Current Gain ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 8\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	8 6	– –	40 30	
Collector-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$) ($I_C = 12\text{ Adc}$, $I_B = 3\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	– – – –	– – – –	1 1.5 3 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	– – –	– – –	1.2 1.6 1.5	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product ($I_C = 500\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	f_T	4	–	–	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	–	180	–	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 125 Vdc, I _C = 8 A, I _{B1} = I _{B2} = 1.6 A, t _p = 25 μs, Duty Cycle ≤ 1%)	t _d	–	0.06	0.1	μs
Rise Time		t _r	–	0.45	1	μs
Storage Time		t _s	–	1.3	3	μs
Fall Time		t _f	–	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I _C = 8 A, V _{clamp} = 300 Vdc, I _{B1} = 1.6 A, V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _{sv}	–	0.92	2.3	μs
Crossover Time		t _c	–	0.12	0.7	μs

2. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

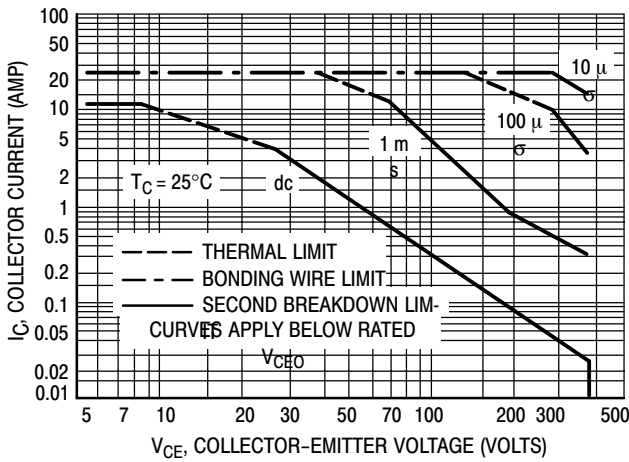


Figure 1. Forward Bias Safe Operating Area

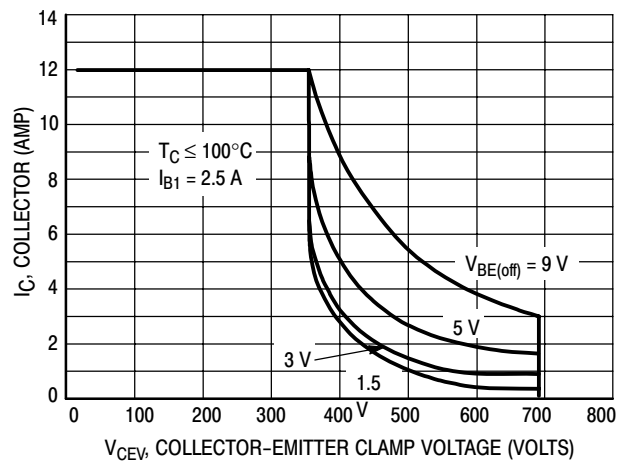


Figure 2. Reverse Bias Switching Safe Operating Area

The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

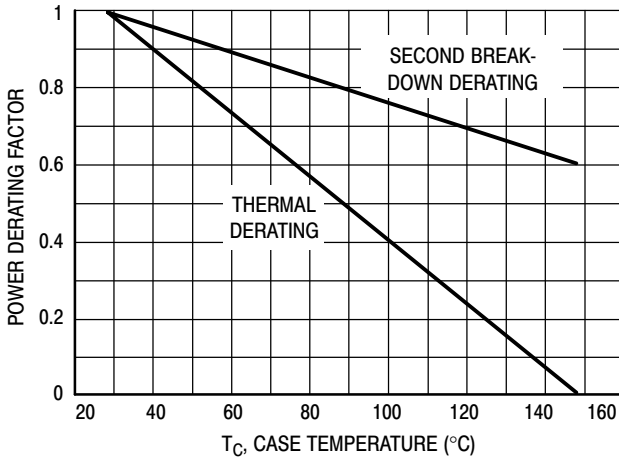


Figure 3. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

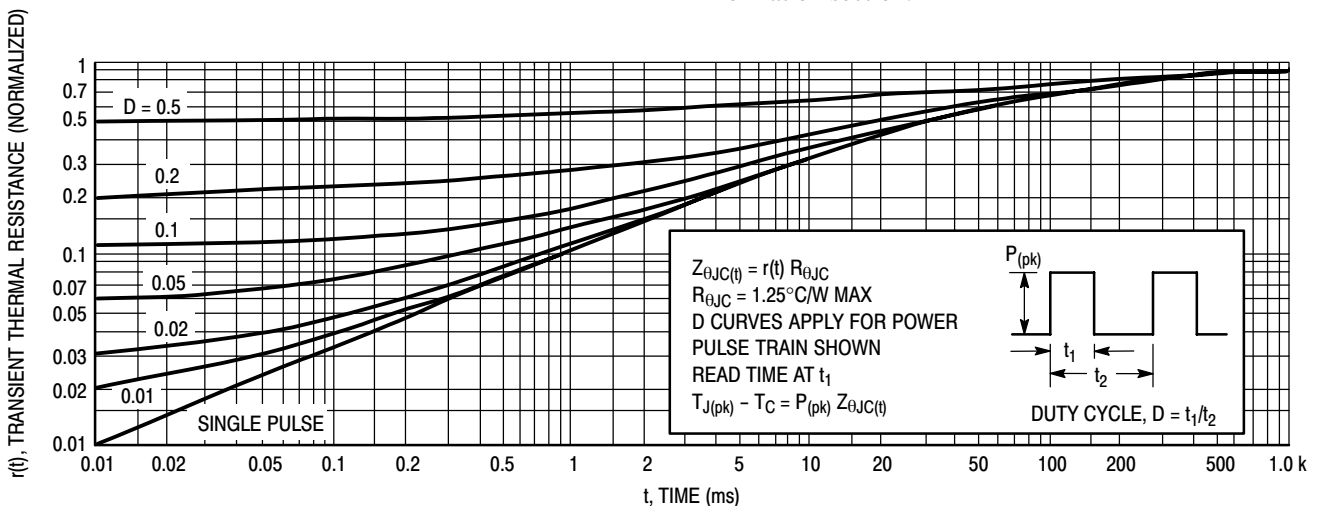


Figure 4. Typical Thermal Response [$Z_{\theta JC}(t)$]

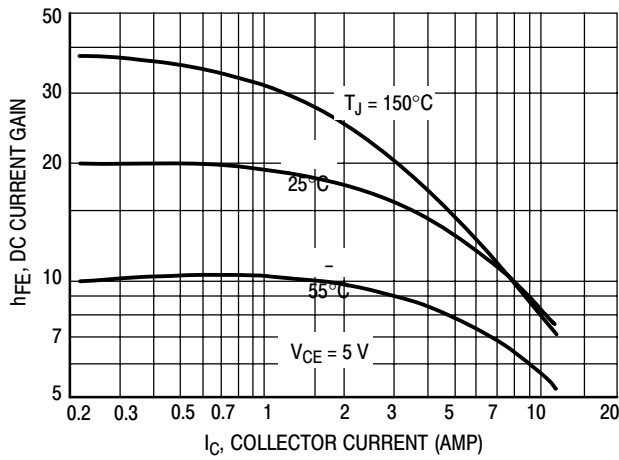


Figure 5. DC Current Gain

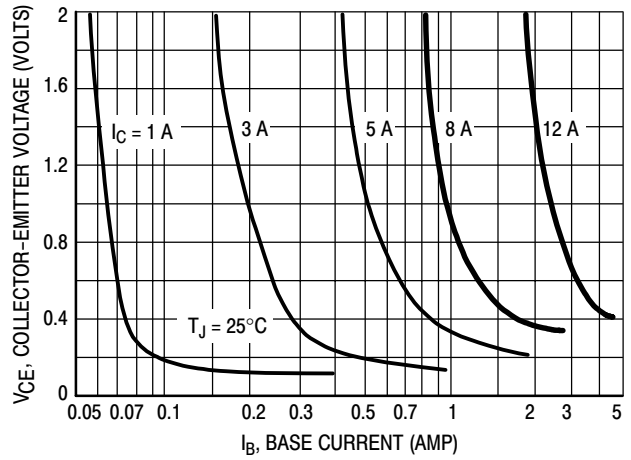


Figure 6. Collector Saturation Region

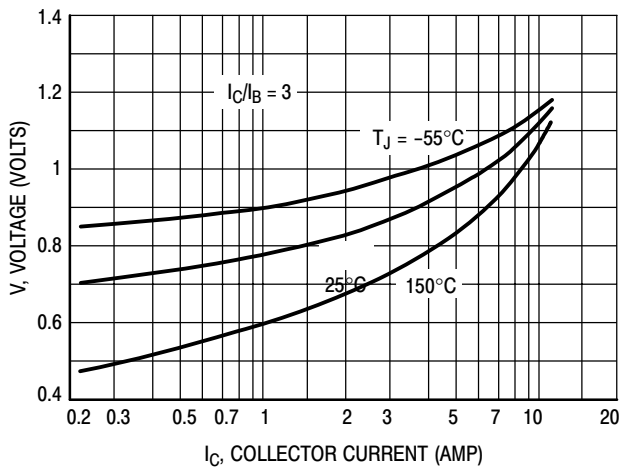


Figure 7. Base-Emitter Saturation Voltage

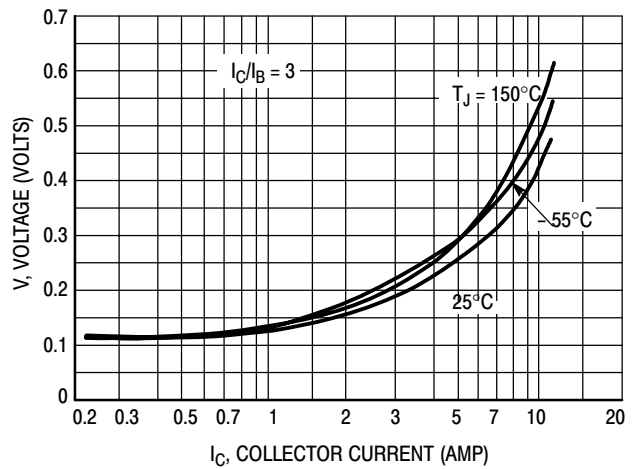


Figure 8. Collector-Emitter Saturation Voltage

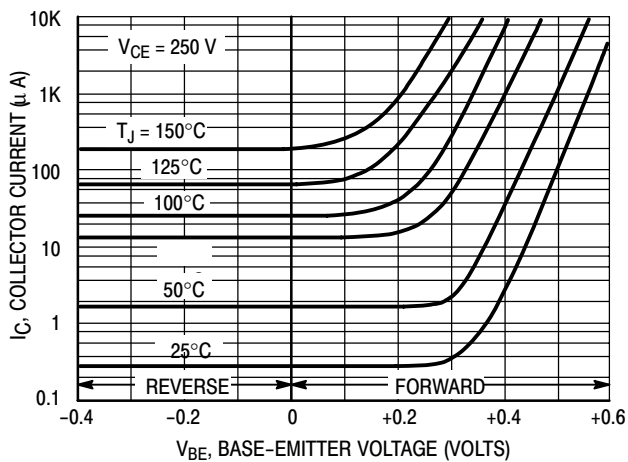


Figure 9. Collector Cutoff Region

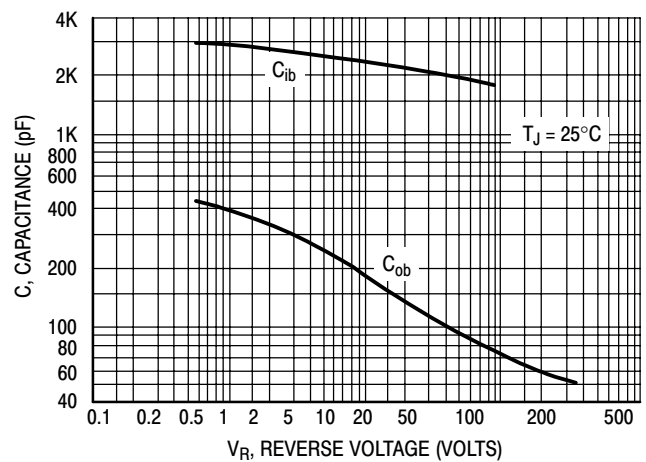
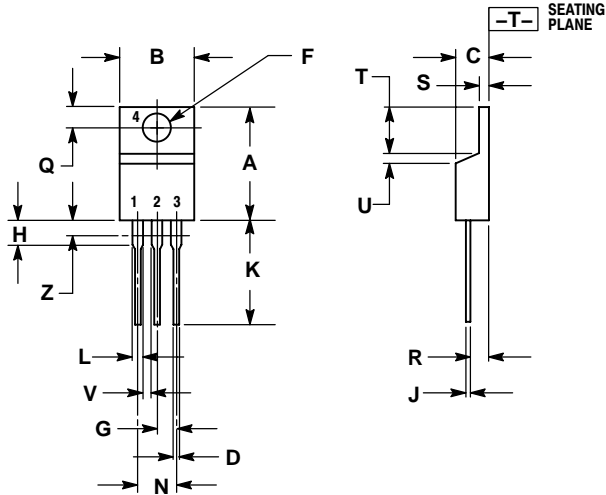


Figure 10. Capacitance

MJE13009

PACKAGE DIMENSIONS

TO-220AB CASE 221A-09 ISSUE AA



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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